82062
WINCHESTER DISK CONTROLLER

- **Controls ST506/ST412 Interface Winchester Drives**
- **5 MBit/Sec Transfer Rate**
- **128, 256, 512, and 1024 Byte Sector Lengths**
- **Six High-Level Commands: Restore, Seek, Read Sector, Write Sector, Scan ID, and Write Format**
- **Multiple Sector Transfer Capability**
- **Implied Seek With Read/Write Commands**
- **7 Byte Sector Length Extension For External Error Correction Code**
- **Single +5 Volt Power Supply**

The 82062 Winchester Disk Controller (WDC) device interfaces microprocessor systems to Winchester Disks that use the Seagate Technology ST506/ST412 interface. Examples include the Seagate ST506 and ST412, Shugart SA604 and SA606, Tandon 600, and Computer Memories CM5206 and CM5412. The device translates parallel data from the microprocessor to a 5 mbit/sec, MFM-encoded serial bit stream. It provides all of the drive control logic and, in addition, control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The 82062 is designed to interface to the host controller through an external sector buffer.

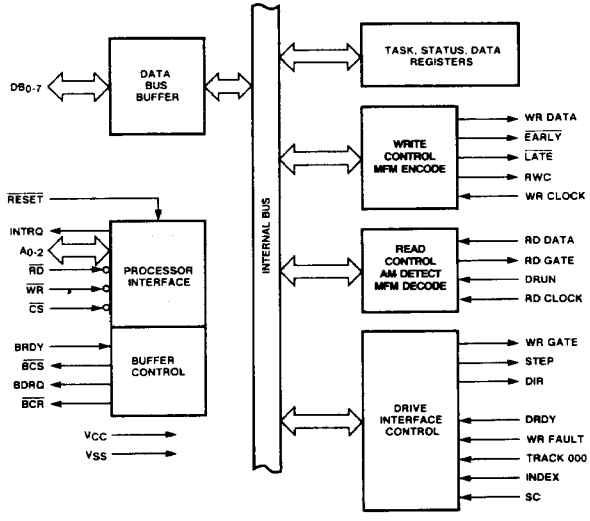

Figure 1. 82062 Block Diagram

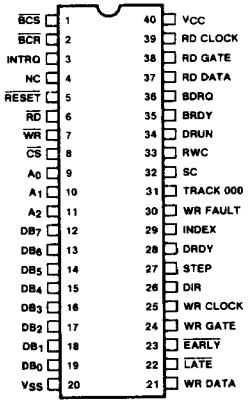

Figure 2. Pin Configuration

ORDER NUMBER 210446-005

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
$\overline{BCS}$	1	O	**Buffer Chip Select:** Output used to enable reading or writing of the external sector buffer by the 82062. When low, the host should not able to drive the 82062 data bus, $\overline{RD}$, or $\overline{WR}$ lines.
$\overline{BCR}$	2	O	**Buffer Counter Reset:** Output that is strobed by the 82062 prior to read/write operation. This pin is strobed whenever $\overline{BCS}$ changes state. Used to reset the address counter of the buffer memory.
INTRQ	3	O	**Interrupt Request:** Interrupt generated by the 82062 upon command termination. It is reset when any register is read. Optionally signifies when a data transfer is required on Read Sector commands.
N/C	4		No connection. Reserved for future use.
$\overline{RESET}$	5	I	**Reset:** Initializes the controller and clears all status flags. Does not clear the Task Registers.
$\overline{RD}$	6	I/O	**Read:** As an input, $\overline{RD}$ controls the transfer of information from the 82062 registers to the host. $\overline{RD}$ is an output when the 82062 is reading data from the sector buffer ($\overline{BCS}$ low).
$\overline{WR}$	7	I/O	**Write:** As an input, $\overline{WR}$ controls the transfer of command or task information into the 82062 registers. $\overline{WR}$ is an output when the 82062 is writing data to the sector buffer ($\overline{BCS}$ low).
$\overline{CS}$	8	I	**Chip Select:** Enables $\overline{RD}$ and $\overline{WR}$ as inputs for access to the Task Registers. It has no effect once a disk command starts..
A_0-A_2	9-11	I	**Address:** Used to select a register from the task register file.
DB_0-DB_7	12-19	I/O	**Data Bus:** Bidirectional 8-bit Data Bus with control determined by $\overline{BCS}$. When $\overline{BCS}$ is high the microprocessor has full control of the data bus for reading and writing the Task Registers. When $\overline{BCS}$ is low the 82062 controls the data bus to transfer data to or from the buffer.
GND	20		**Ground**
WR DATA	21	O	**Write Data:** Open drain output that shifts out MFM data at a rate determined by Write Clock. Requires an external flip-flop clocked at 10 MHz. See note 1.
$\overline{LATE}$	22	O	**Late:** Open drain output used to derive a delay value for write precompensation. Valid when WR GATE is high. Active on all cylinders. See note 1.
$\overline{EARLY}$	23	O	**Early:** Open drain output used to derive a delay value for write precompensation. Valid when WR GATE is high. Active on all cylinders. See note 1.
WR GATE	24	O	**Write Gate:** High when write data is valid. WR GATE goes low if the WR FAULT input is active. This output is used by the drive to enable head write current.
WR CLOCK	25	I	**Write Clock:** Clock input used to derive the write data rate. Frequency - 5MHz for the ST506 interface, 4.34MHz for the SA 1000 interface. See note 2.
DIR	26	O	**Direction:** High level on this output tells the drive to move the head inward (increasing cylinder number). The state of this signal is determined by the 82062's internal comparison of actual cylinder location vs desired cylinder.
STEP	27	O	**Step:** Provides 8.4 microsecond pulses to move the drive head to another cylinder at a programmable frequency.
DRDY	28	I	**Drive Ready:** If DRDY from the drive goes low, the command will be terminated.

Table 1. Pin Description (continued)

Symbol	Pin No.	Type	Name and Function
INDEX	29	I	**Index:** Signal from the drive indicating the beginning of a track. It is used by the 82062 during formatting, and for counting retries. Index is edge triggered. Only the rising edge is valid.
WR FAULT	30	I	**Write Fault:** An error input to the 82062 which indicates a fault condition at the drive. If WR FAULT from the drive goes high, the command will be terminated.
TRACK 000	31	I	**Track Zero:** Signal from the drive which indicates that the head is at the outermost cylinder. Used by the Restore command.
SC	32	I	**Seek Complete:** Signal from the drive indicating to the 82062 that the drive head has settled and that reads or writes can be made. SC is edge triggered. Only the rising edge is valid.
RWC	33	O	**Reduced Write Current:** Signal goes high for all cylinder numbers above the value programmed in the Write Precomp Cylinder register. It is used by the precompensation logic and by the drive to reduce the effects of bit shifting.
DRUN	34	I	**Data Run:** This signal informs the 82062 when a field of ones or zeroes has been detected in the read data stream by an external one-shot. This indicates the beginning of an ID field. RD GATE is brought high when DRUN is sampled high for 16 clock periods. See note 2.
BRDY	35	I	**Buffer Ready:** Input used to signal the controller that the buffer is ready for reading (full), or writing (empty), by the host uP. Only the rising edge indicates the condition.
BDRQ	36	O	**Buffer Data Request:** Activated during Read or Write commands when a data transfer between the host and the 82062's sector buffer is required. Typically used as a DMA request line, or to generate an interrupt.
RD DATA	37	I	**Read Data:** Single ended input that accepts MFM data from the drive. See note 2.
RD GATE	38	O	**Read Gate:** Output that is high for data and ID fields. Goes active when DRUN has been high for 16 WR CLOCK periods to permit the external phase lock loop to lock onto the incoming disk data stream.
RD CLOCK	39	I	**Read Clock:** Clock input derived from the external data recovery circuits. See note 2.
V_{cc}	40	I	**D.C. Power:** +5V

Note 1: This pin requires a pull-up resistor to function properly. A value of 1000 ohms will work satisfactorily.

Note 2: This pin requires input levels that are not TTL compatible. These lines can be interfaced to TTL with a pull-up resistor. Too small of a resistor will produce a VIL level that is too high. Too large of a resistor will degrade the signal's rise time. A minimum value for the resistor is determined as follows:

$$\frac{(V_{CC}\ \text{max}) - (82062\ V_{IL}\ \text{max})}{(\text{TTL}\ I_{OL}\ \text{min}) - (82062\ I_{IL}\ \text{max})}$$

This would typically be:

$$\frac{5.25V - 0.5V}{1.6\ mA - 10\ \mu A} \simeq 3k\ \Omega$$

FUNCTIONAL DESCRIPTION

The Intel 82062 Winchester Disk Controller (WDC) integrates much of the logic needed to implement Winchester Disk controller subsystems. It provides MFM-encoded data and all the control lines required by hard disks using the Seagate Technology ST506 or Shugart Associates SA1000 interface standard. Currently, most 5¼ inch and many 8 inch Winchester Drives use this interface.

Due to the higher data rates required by these drives—1 byte every 1.6 usec—the 82062 is designed to interface with the host CPU or I/O controller through an external buffer RAM. The 82062 WDC has four pins that minimize the logic required to design a buffer interface.

Figure 3 shows a block diagram of an 82062 subsystem. The WDC is controlled by the host CPU through six commands:

Restore
Seek
Read Sector
Write Sector
Scan ID
Write Format

These commands use information stored by six task registers. Command execution starts immediately after the command register is loaded—therefore commands require only one byte from the CPU after the WDC has been initialized.

The 82062 adds all the required track formatting to the data field, including two bytes of CRC. Optionally, these two bytes can be replaced by seven bytes of ECC information for external error correction.

INTERNAL ARCHITECTURE

The internal architecture of the 82062 WDC is shown in more detail in Figure 4. The major functional blocks are:

PLA Controller

The PLA interprets commands and provides all control functions. It is synchronized with WR CLOCK.

Magnitude Comparator

A 10-bit magnitude comparator is used to calculate the direction and number of step pulses needed to move the head from the present to the desired cylinder.

CRC Logic

Generates and checks the cyclic redundancy check characters appended to the ID and data fields. The polynomial used is:

$$X^{16} + X^{12} + X^5 + 1.$$

MFM Encode/Decode

Encodes and decodes MFM data to be written/read from the drive. The MFM encoder operates from WR CLOCK, a clock having a frequency equivalent to the bit rate. The MFM decoder operates from RD CLOCK, a bit rate clock generated from the external data separator. RD CLOCK and WR CLOCK need not be synchronized.

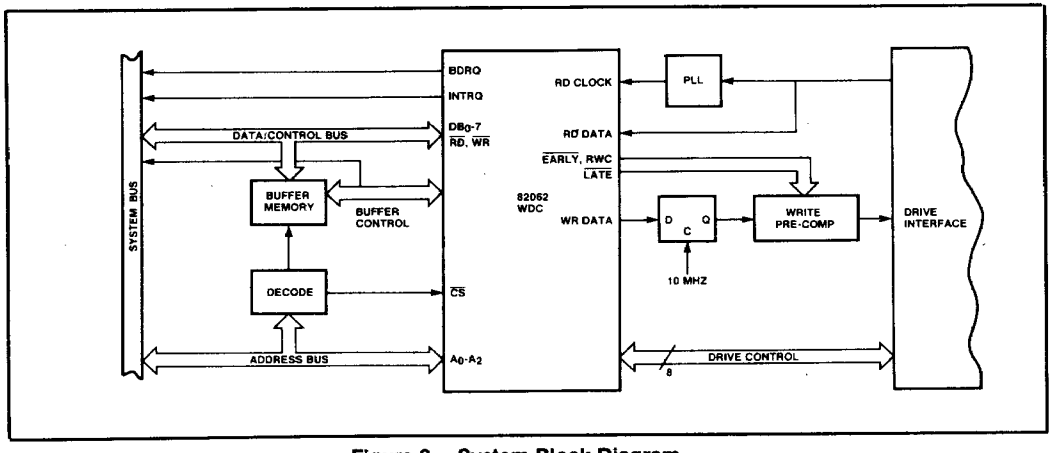

Figure 3. System Block Diagram

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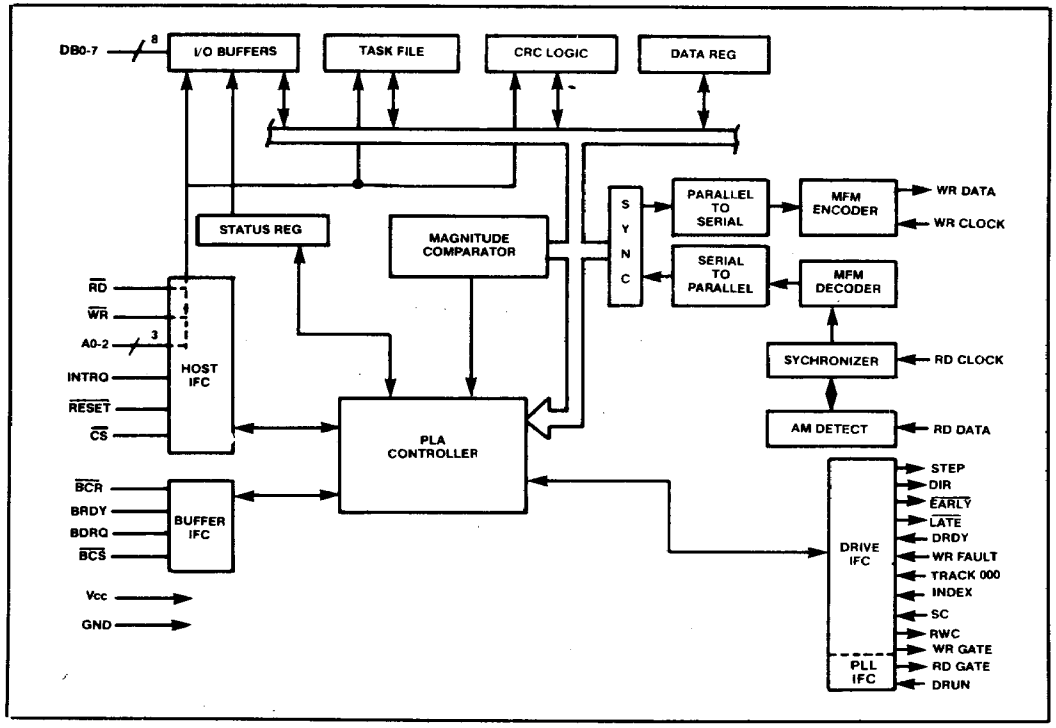

Figure 4. 82062 Detailed Block Diagram

AM Detect

The address mark detector checks the incoming data stream for a unique missing clock pattern (Data = A1H, Clock = 0AH) used in each ID and data field.

Host/Buffer Interface Control

The Host/Buffer IFC logic contains all of the necessary circuitry to communicate with the 8-bit bus from the host processor.

Drive Interface Control

The Drive IFC logic controls and monitors all lines from the drive, with the exception of read and write data.

DRIVE INTERFACE

The drive side of the 82062 WDC requires three sections of external logic. These are buffer/receivers, data separator, and write precompensation. Figure 5 illustrates a drive side interface.

The buffer/receivers condition the control lines to be driven down the cable to the drive. The control lines are typically single-ended, resistor terminated TTL levels. The data lines to and from the drive also require buffering, but are differential RS-422 levels. The interface specification to the drive can be found in the manufacturers' OEM manual. The WDC supplies TTL compatible signals, and will interface to most buffer/driver devices.

The data recovery circuits consist of a phase-lock loop data separator and associated components. The 82062 WDC interacts with the data separator thru the DATA RUN (DRUN) and RD GATE signals. A block diagram of a typical data separator circuit is shown in Figure 6. Read data from the drive is presented to the RD DATA input of the WDC, the reference multiplexor, and a retriggerable one-shot. The RD GATE (Pin 38) output will be low when the WDC is not inspecting data. The PLL at this time should remain locked to the reference clock.

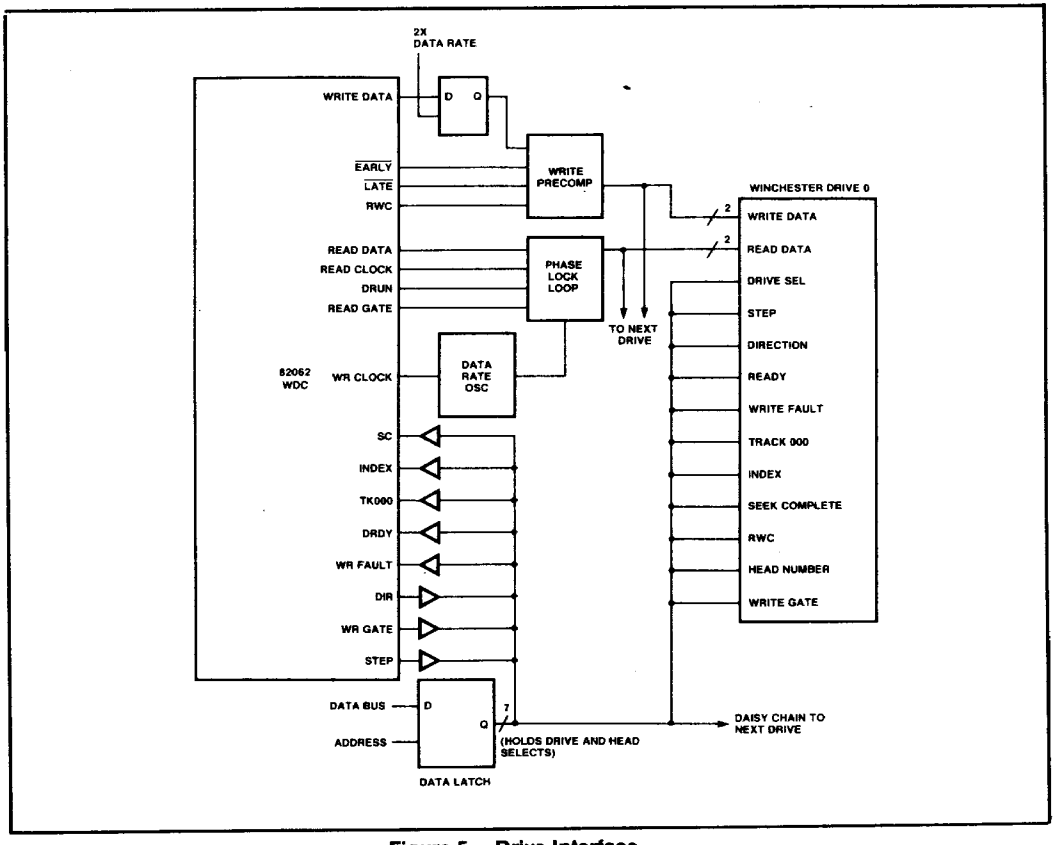

Figure 5. Drive Interface

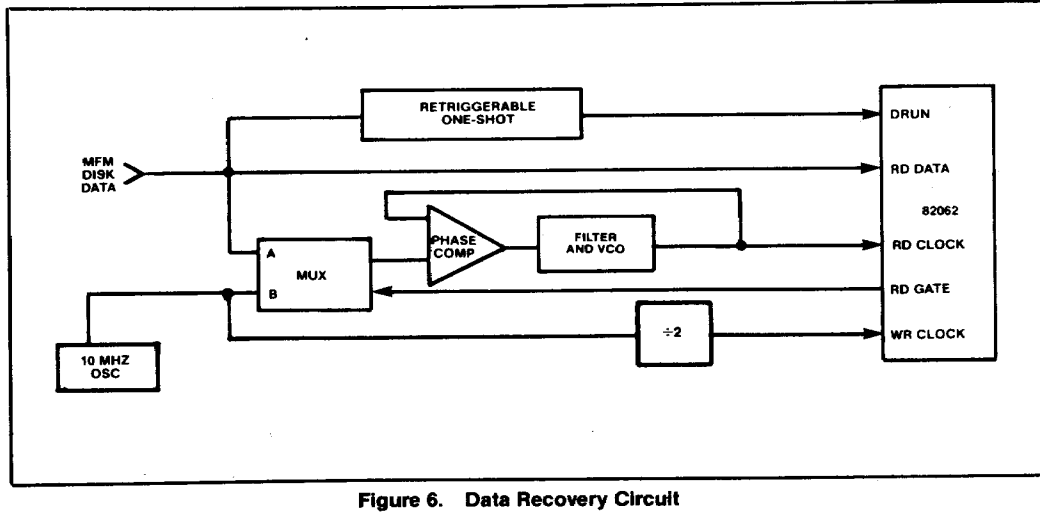

Figure 6. Data Recovery Circuit

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When any Read/Write command is initiated and a search for address mark begins, the DRUN input is examined. The DRUN one-shot is set for slightly greater than one bit time, allowing it to retrigger constantly on a field of ones and zeros. An internal counter times out to see that DRUN is high for 2 byte times. RD GATE is set by the WDC, switching the data separator to lock onto the incoming data stream. If DRUN falls prior to an additional 7 byte times, RD GATE is lowered and the process is repeated. RD GATE will remain active high until a non-zero, non-address mark byte is detected. It will then lower RD GATE for two byte times (to allow the PLL to lock back on to the reference clock), and start the DRUN search again. If an address mark is detected, RD GATE will be held high and the command will continue searching for the proper ID field. This sequence is shown in the flow chart in Figure 7.

The write precompensation logic is controlled by the signals REDUCE WRITE CURRENT (RWC), $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$. The cylinder in which the RWC line becomes active is controlled by the REDUCE WRITE CURRENT register in the Task Register File. It can be used to turn on the precomp circuitry on a predetermined cylinder. If the REDUCE WRITE CURRENT register contents are FFH, then RWC will always be low.

The signals $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ are used to tell the precomp circuitry how much delay is required on the WR DATA pulse about to be sent. The amount of delay is determined externally through a digital delay line or equivalent circuitry. Since the $\overline{\text{EARLY}}$ signal occurs after the fact, WR DATA should be delayed by one interval when both $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ are deasserted, two intervals when $\overline{\text{LATE}}$ is asserted, and no delay when $\overline{\text{EARLY}}$ is asserted. An interval is, for example, 12-15 ns. for the ST506 interface. $\overline{\text{EARLY}}$ or $\overline{\text{LATE}}$ will be active slightly ahead of the WR DATA pulse. $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ will never be asserted at the same time. $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ are always active, and should be gated externally by the RWC signal.

HOST PROCESSOR INTERFACE

The primary interface between the host processor and the 82062 WDC is through an 8-bit bi-directional data bus. This bus is used to transmit/receive data to both the WDC and a sector buffer. The sector buffer is constructed with either FIFO memory, or static RAM and a counter. Since the WDC will use the data bus when accessing the sector buffer, a transceiver must be used to isolate the host during this time. Figure 8 shows a typical connection to a sector buffer implemented with RAM memory. Whenever the WDC is not using the sector buffer, The BUFFER CHIP SELECT ($\overline{\text{BCS}}$) is high (disabled). This allows the host to access the WDC's Task Register File, and

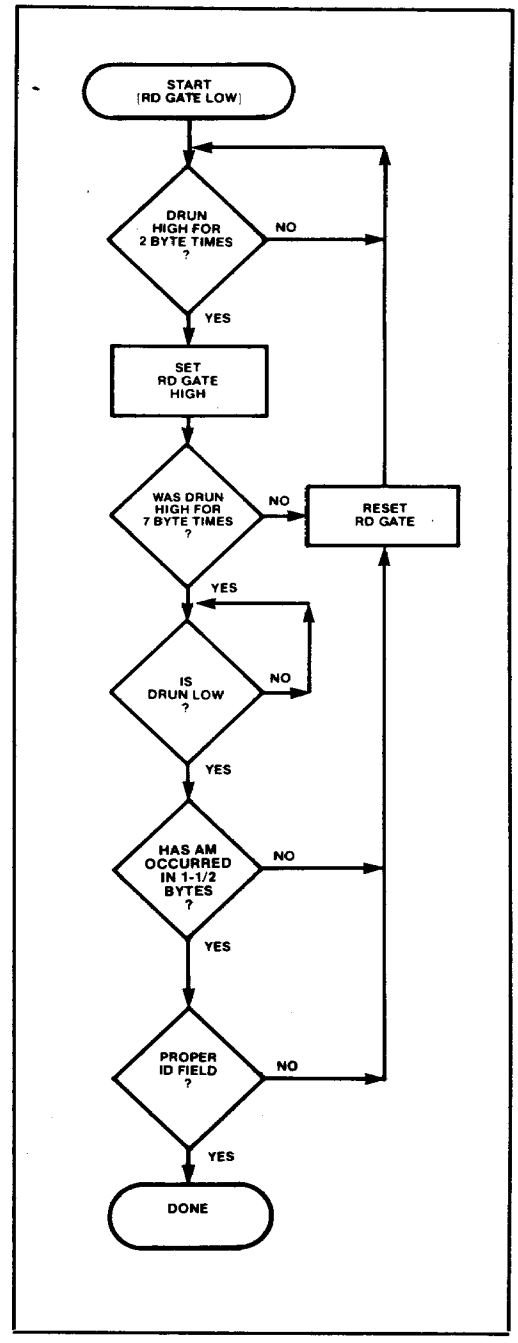

Figure 7. PLL Control Sequence

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to set up parameters prior to issuing a command. It also allows the host to access the RAM buffer. A decoder is used to generate a chip select when A_{0-2} is '000', an unused address in the WDC. A binary counter is enabled whenever $\overline{RD}$ or $\overline{WR}$ go active and is incremented on the trailing edge of the chip select. This allows the host to access sequential bytes within the RAM. The decoder also generates another chip select when A_{0-2} does not equal '000', allowing access to the WDC's internal registers while keeping the RAM tri-stated.

During a WRITE SECTOR command, the host processor sets up data in the Task Register File and then issues the command. It then generates a status to inform the host that it may load the buffer with the data to be written. When the counter reaches its maximum count, the BUFFER READY (BRDY) signal is made active (by the "carry" out of the counter), informing the WDC that the buffer is full. (BRDY is a rising edge triggered signal which will be ignored if activated before the WDC issues $\overline{BCR}$). $\overline{BCS}$ is then made active, disconnecting the host through the transceivers, and the $\overline{RD}$ and $\overline{WR}$ lines become outputs from the WDC to allow it to access the buffer.

When the WDC is done using the buffer, it disables $\overline{BCS}$ which again allows the host to access the local bus. The READ SECTOR command operates in a similar manner, except the buffer is loaded by the WDC instead of the host processor.

Another control signal called BUFFER DATA REQUEST (BDRQ, not used in Figure 8) is a DMA signal that can inform a DMA controller when the 82062 WDC is requesting data. For further explanation, refer to the individual command descriptions and the A.C. Characteristics. In a READ SECTOR command, interrupts are generated at the termination of the command. An interrupt may be specified to occur either at the end of the command, or when BDRQ is activated. The INTERRUPT line (INTRQ) is cleared either by reading the STATUS register, or by writing a new command in the COMMAND register.

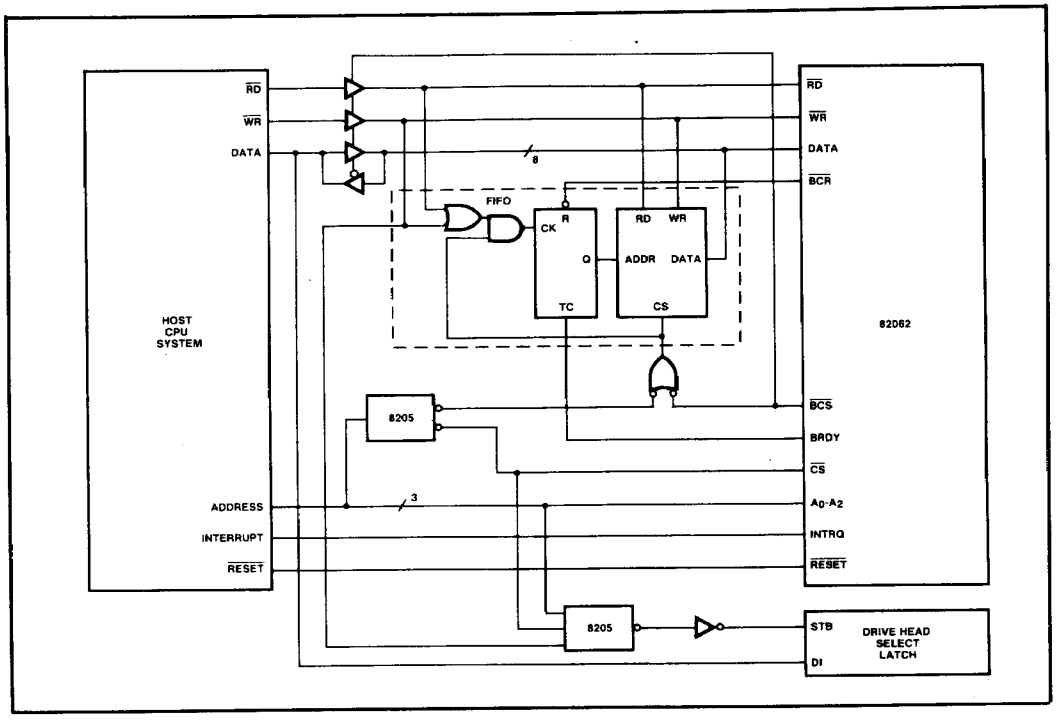

Figure 8. CPU Buffer Interface

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TASK REGISTER FILE

The Task Register File is a bank of registers used to hold parameter information pertaining to each command. These registers and their addresses are:

A2	A1	A0	READ	WRITE
0	0	0	(Bus Tri-Stated)	(Bus Tri-Stated)
0	0	1	Error Flags	Reduce Write Current
0	1	0	Sector Count	Sector Count
0	1	1	Sector Number	Sector Number
1	0	0	Cylinder Low	Cylinder Low
1	0	1	Cylinder High	Cylinder High
1	1	0	SDH	SDH
1	1	1	Status Register	Command Register

NOTE: Registers are not cleared by $\overline{\text{RESET}}$.

ERROR REGISTER

This read-only register contains specific error status after the completion of a command. The bits are defined as follows:

7	6	5	4	3	2	1	0
BBD	CRC	—	ID	—	AC	TK000	DM

Bit 7 - Bad Block Detect

This bit is set when an ID field has been encountered that contains a bad block mark. It is used for bad sector mapping.

Bit 6 - CRC Data Field

This bit is set when a data field CRC error has ocurred. The sector buffer may still be read but will contain errors.

Bit 5 - Reserved Not used.

Forced to zero.

Bit 4 - ID Not Found

This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk, or if an ID field CRC error has occured.

Bit 3 - Reserved Not used.

Forced to zero.

Bit 2 - Aborted Command

This bit is set if a command was issued while DRDY (Pin 28) is deasserted or WR FAULT (Pin 30) is asserted. The Aborted Command bit will also be set if an undefined command is written into the COMMAND register, but an implied seek will be executed.

Bit 1 - TRACK 000

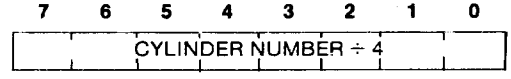
This bit is set only by the RESTORE command. It indicates that TRACK 000 (Pin 31) has not gone active after the issuance of 1024 stepping pulses.

Bit 0 - Data Address Mark

This bit is set during a READ SECTOR command if the Data Address Mark is not found after the proper Sector ID is read.

REDUCE WRITE CURRENT REGISTER

This register is used to define the cylinder number where RWC (Pin 33) is asserted:



The value (0-255) loaded into this register is internally multiplied by 4 to specify the actual cylinder where RWC is asserted. Thus a value of 01H will cause RWC to activate on cylinder 4, 02H on cylinder 8, and so on. RWC switching points are then 0,4,8, . . . 1020. RWC will be asserted when the present cylinder is greater than or equal to the cylinder indicated by this register. For example, the ST506 interface requires precomp on cylinder 128 (80H) and above. Therefore, the REDUCE WRITE CURRENT register should be loaded with 32 (20H). A value of FFH will make RWC stay low, regardless of the actual cylinder number.

SECTOR COUNT REGISTER

This register is used to define the number of sectors that need to be transfered to the buffer during a READ MULTIPLE SECTOR or WRITE MULTIPLE SECTOR command.:

7	6	5	4	3	2	1	0
# OF SECTORS							

The value contained in the register is decremented after each sector is transferred to/from the sector buffer. A zero represents a 256 sector transfer, a one a 1 sector transfer, etc. This register is a "don't care" when single sector commands are specified.

SECTOR NUMBER

This register holds the sector number of the desired sector:

7	6	5	4	3	2	1	0
SECTOR NUMBER							

For a multiple sector command, it specifies the first sector to transferred. It is incremented after each sector is transferred to/from the sector buffer. The SECTOR NUMBER register may contain any value from 0 to 255.

The SECTOR NUMBER register is also used to program the Gap 1 and Gap 3 lengths to be used when formatting a disk. See the WRITE FORMAT command description for further explanation.

CYLINDER NUMBER LOW REGISTER

This register holds the lower byte of the desired cylinder number:

7	6	5	4	3	2	1	0
LS BYTE OF CYLINDER NUMBER							

It is used in conjunction with the CYLINDER NUMBER HIGH register to specify a range of 0 to 1023.

CYLINDER NUMBER HIGH REGISTER

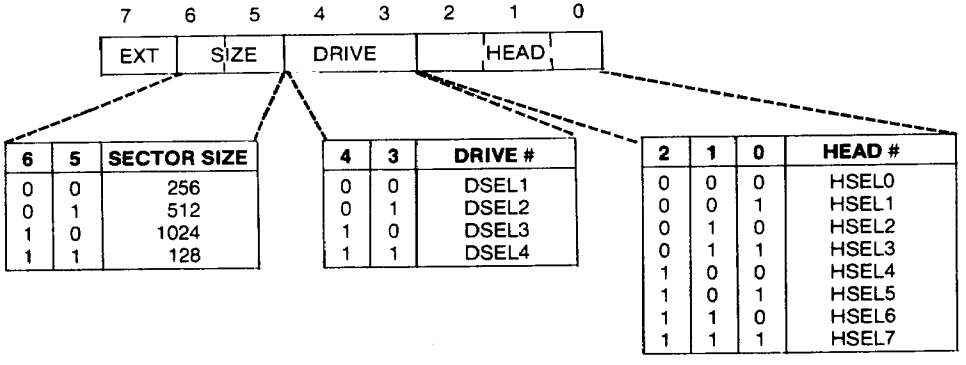
This register holds the two most significant bits of the desired cylinder number:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	(9)	(8)

Internal to the 82062 WDC is another pair of registers that hold the actual position where the R/W heads are located. The CYLINDER NUMBER HIGH and LOW registers can be considered the cylinder destination for seeks and other commands. After these commands are executed, the internal cylinder position registers' contents are equal to the cylinder high/low registers. If a drive number change is detected on a new command, the WDC automatically reads an ID field to update its internal cylinder position registers. This affects all commands except a RESTORE.

SECTOR/DRIVE/HEAD REGISTER

The SDH register contains the desired sector size, drive number, and head number parameters. The format is diagramed below.



6	5	SECTOR SIZE
0	0	256
0	1	512
1	0	1024
1	1	128

4	3	DRIVE #
0	0	DSEL1
0	1	DSEL2
1	0	DSEL3
1	1	DSEL4

2	1	0	HEAD #
0	0	0	HSEL0
0	0	1	HSEL1
0	1	0	HSEL2
0	1	1	HSEL3
1	0	0	HSEL4
1	0	1	HSEL5
1	1	0	HSEL6
1	1	1	HSEL7

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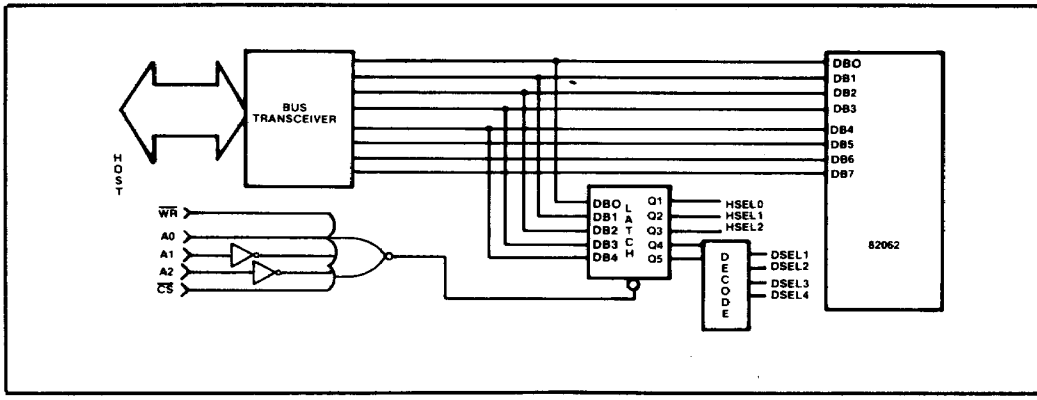


Figure 9. Drive/Head Select Logic

Both head number and sector size are compared against the disks' ID field. Head select and drive select lines are not available as outputs from the 82062 WDC and must be generated externally. Figure 9 shows a possible logic implementation of these select lines.

Bit 7, the extension bit (EXT), is used to extend the data field by seven bytes when using ECC codes. When EXT = 1, the CRC is not appended to the end of the data field, the data field becomes "sector size + 7" bytes long. The CRC is checked on the ID field regardless of the state of EXT. Note that the sector size bits (SIZE) are written to the ID field during a formatting command. The SDH byte written into the ID field is different than the SDH Register contents. The recorded SDH byte does not have the drive number (DRIVE) written but does have the BAD BLOCK mark written. The format is:

7	6	5	4	3	2	1	0
BAD BLOCK	SIZE		0	0		HEAD #	

Note that use of the extension bit requires the gap lengths to be modified as described in the WRITE FORMAT command description.

STATUS REGISTER

The status register is a read-only register which informs the host of certain events performed by the 82062 WDC as well as reporting status from the drive control lines. The INTRQ line will be reset when the status register is read. The format is:

7	6	5	4	3	2	1	0
BUSY	READY	WF	SC	DRQ	—	CIP	ERROR

Bit 7 - Busy

This bit is set whenever the 82062 WDC is accessing the disk. Commands should not be loaded into the COMMAND register while Busy is set. Busy is set when a command is written into the WDC and is cleared at the end of all commands except READ SECTOR. While executing a READ SECTOR command, Busy is cleared after the sector buffer has been filled. When the Busy bit is set, no other bits in either the STATUS or any other registers are valid.

Bit 6 - Ready

This bit reflects the state of the DRDY (Pin 28) line.

Bit 5 - Write Fault

This bit reflects the state of the WR FAULT (Pin 30) line. Whenever WR FAULT goes high, an interrupt will be generated.

Bit 4 - Seek Complete

This bit reflects the state of the SC (Pin 32) line. Commands which initiate a seek will pause until Seek Complete is set.

Bit 3 - Data Request

The Data request bit (DRQ) reflects the state of the BDRQ (Pin 36) line. It is set when the sector buffer should be loaded with data or read by the host processor, depending upon the command. The DRQ bit and the BDRQ line remain high until BRDY is sensed, indicating the operation is completed. BDRQ can be used in DMA interfacing, while DRQ can be used for programmed I/O transfers.

Bit 2 - Reserved

Not Used. Forced to zero.

Bit 1 - Command in Progress

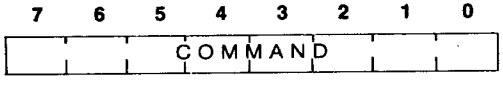
When this bit is set, a command is being executed and a new command should not be loaded until it is cleared. Although a command may be executing, the sector buffer is still available for access by the host processor. Only the STATUS register may be read. If other registers are read, the STATUS register contents will be returned.

Bit 0 - Error

This bit is set whenever any bits in the ERROR register are set. It is the logical 'or' of the bits in the error register and may be used by the host processor to quickly check for successful completion of a command. This bit is reset when a new command is written into the COMMAND register.

COMMAND REGISTER

This write-only register is loaded with the desired command:



The command begins to execute immediately upon loading. This register should not be loaded while the Busy or Command in Progress bits are set in the STATUS register. The INTRQ line (Pin 3), if set, will be cleared by a write to the COMMAND register.

INSTRUCTION SET

The 82062 WDC instruction set contains six commands. Prior to loading the command register, the host processor must first set up the Task Register File with the information needed for the command. Except for the COMMAND register, the registers may be loaded in any order. If a command is in progress, a subsequent write to the COMMAND register will be ignored until execution of the current command is completed as indicated by the command in progress bit in the STATUS register being cleared

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	R3	R2	R1	R0
SEEK	0	1	1	1	R3	R2	R1	R0
READ SECTOR	0	0	1	0	I	M	0	T
WRITE SECTOR	0	0	1	1	0	M	0	T
SCAN ID	0	1	0	0	0	0	0	T
WRITE FORMAT	0	1	0	1	0	0	0	0

R_{3-0} = Rate Field

For 5 MHz WR CLOCK:

R_{3-0} =	0000 -	≈35 us
	0001 -	0.5 ms
	0010 -	1.0 ms
	0011 -	1.5 ms
	0100 -	2.0 ms
	0101 -	2.5 ms
	0110 -	3.0 ms
	0111 -	3.5 ms
	1000 -	4.0 ms
	1001 -	4.5 ms
	1010 -	5.0 ms
	1011 -	5.5 ms
	1100 -	6.0 ms
	1101 -	6.5 ms
	1110 -	7.0 ms
	1111 -	7.5 ms

T = Retry Enable

T = 0	Enable Retries
T = 1	Disable Retries

M = Multiple Sector Flag

M = 0	Transfer 1 Sector
M = 1	Transfer Multiple Sectors

I = Interrupt Enable

I = 0	Interrupt at BDRQ time
I = 1	Interrupt at end of command

RESTORE COMMAND

The RESTORE command is usually used on a power-up comdition. The actual stepping rate used for the RESTORE is determined by the Seek Complete time. A step pulse is issued and the 82062 WDC waits for a rising edge on the Seek Complete (SC) line before issuing the next pulse. If 10 index pulses are received without a rising edge of SC, the 82062 will switch to sensing the level of the SC line. If after 1,024 stepping pulses the TRACK 000 line does not go active, the WDC will set the TRACK 000 bit in the ERROR register and terminate with an INTRQ. An interrupt will also occur if WR FAULT goes active or DRDY goes inactive at any time during execution.

The rate field specified R_{3-0} is stored in an internal register for future use in commands with implied seeks.

A flowchart of the RESTORE command is shown in Figure 10.

SEEK COMMAND

Since all commands except the SCAN ID command feature an implied seek, the SEEK command can be used for overlap seek operations on multiple drives. The actual stepping rate used is taken from the Rate Field of the command, and is stored in an internal register for future use. If DRDY goes inactive or WR FAULT goes active at any time during the seek, the command is terminated and an INTRQ is generated.

The direction and number of step pulses needed is calculated by comparing the contents of the CYLINDER NUMBER LOW/HIGH register pair to the internal cylinder position register. After all steps have been issued, the internal cylinder position register is updated and the command is terminated. The Seek Complete (SC) line is not checked at the beginning or end of the command.

If an implied seek was performed, the 82062 will search until a rising edge of SC is received. If 10 index pulses are received without a rising edge of SC, the 82062 will switch to sensing the level of the SC line.

A flowchart of the SEEK command is shown in Figure 11.

READ SECTOR

The READ SECTOR command is used to transfer one or more sectors of data from the disk to the sector buffer. Upon receipt of the READ SECTOR command, the 82062 WDC checks the CYLINDER NUMBER LOW/HIGH register pair against the internal cylinder position register to see if they are equal. If not, the direction and number of steps calculation is performed and a seek takes place. If an implied seek was performed, the WDC will search until a rising edge of SC is received. The WR FAULT and DRDY lines are monitored throughout the command.

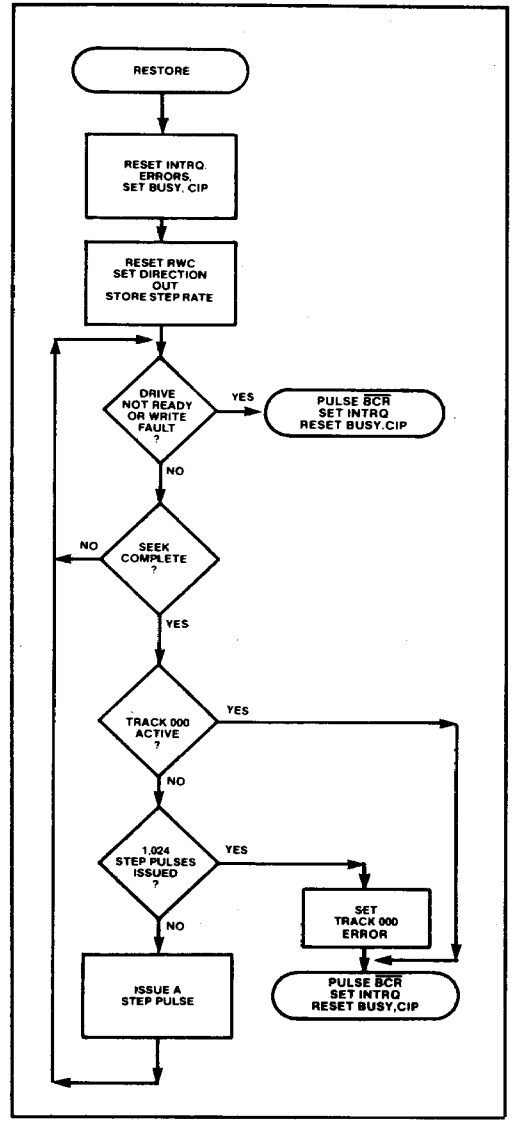


Figure 10. Restore Command Flow

When the Seek Complete (SC) line is high (with or without an implied seek having occured), the search for an ID field begins. If T = 0 (retries enabled), the 82062 WDC must find an ID with the correct cylinder number, head, sector size and CRC within 10 revolutions, or an automatic scan ID will be performed to obtain cylinder position information, and then a seek performed (if necessary). The search for the proper ID will be retried for up to 10 revolutions. If the correct sector is still not found, the appropriate error bits will be set and the command terminated. Data CRC errors will also be retried for up to 10 revolutions (if T = 0).

If T = 1 (retries disabled), the ID search must find the correct sector within 2 revolutions or the appropriate error bits will be set and the command terminated.

Both the READ SECTOR and WRITE SECTOR commands feature a "simulated completion" to ease programming. DRQ/BDRQ will be generated upon detecting an error condition. This allows the same program flow for successful or unsuccessful completion of a command.

When the data address mark is found, the WDC is ready to transfer data to the sector buffer. After the data has been transferred, the I bit is checked. If I = 0, INTRQ is made active coincident with BDRQ, indicating that a transfer of data from the buffer to the host processor is required. If I = 1, INTRQ will occur at the end of the command, i.e. after the buffer is unloaded by the host.

An optional M bit may be set for multiple sector transfers. When M = 0, one sector is transferred and the SECTOR COUNT register is ignored. When M = 1, multiple sectors are transferred. After each sector is transferred the 82062 decrements the SECTOR COUNT register and increments the SECTOR NUMBER register. The next logical sector will be transferred regardless of any interleave. Sectors are numbered at format time by a byte in the ID field.

For the 82062 to make multiple sector transfers to the buffer, the BRDY line must be toggled low to high for each sector. Transfers will continue until the SECTOR COUNT register equals zero, or the BRDY line goes active. If the SECTOR COUNT register is nonzero (indicating more sectors are to be transferred but the buffer is full), BDRQ will be made active and the host must unload the buffer. After this occurs, the buffer will again be free to accept the remaining sectors from the WDC. This scheme enables the user to transfer more sectors than the buffer memory has capacity for.

In summary then, READ SECTOR operation is as follows:

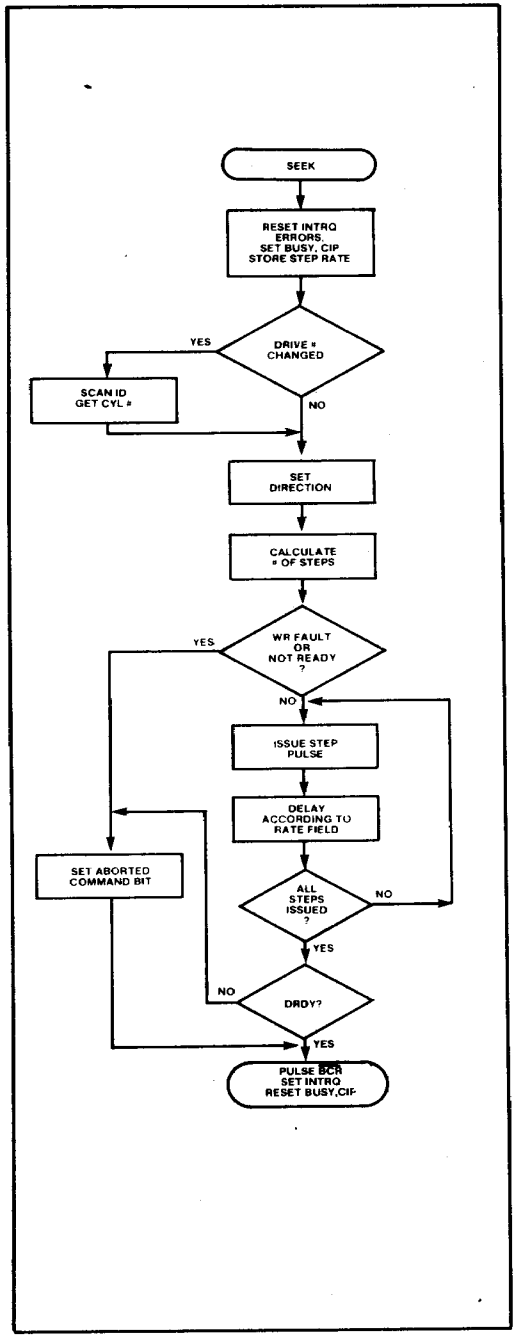


Figure 11. Seek Command Flow

When M = 0 (READ SECTOR)

(1)	**Host:**	Sets up parameters; issues READ SECTOR command.
(2)	**82062:**	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 0.
(3)	**82062:**	Finds sector specified; transfers data to buffer.
(4)	**82062:**	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1.
(5)	**82062:**	Sets BDRQ = 1, DRQ = 1.
(6)	**82062**	If I bit = 1 then go to (9).
(7)	**Host:**	Reads contents of sector buffer.
(8)	**82062:**	Waits for BRDY, then sets INTRQ = 1; END.
(9)	**82062:**	Sets INTRQ = 1.
(10)	**Host:**	Reads out contents of buffer; END.

When M = 1 (READ MULTIPLE SECTOR)

(1)	**Host:**	Sets up parameters; issues READ SECTOR command.
(2)	**82062:**	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 0.
(3)	**82062:**	Finds sector specified; transfers data to buffer.
(4)	**82062:**	Decrements SECTOR COUNT register; increments SECTOR NUMBER register.
(5)	**82062:**	Strobes $\overline{BCR}$; sets $\overline{BCS}$ = 1.
(6)	**82062:**	Sets BDRQ = 1, DRQ = 1.
(7)	**Host:**	Reads out contents of buffer;
(8)	**Buffer:**	Indicates data has been transferred by activating BRDY.
(9)	**82062:**	When BRDY = 1, if Sector Count = 0, then go to (11).
(10)	**82062:**	Go to (2).
(11)	**82062:**	Set INTRQ = 1; END.

A flowchart of the READ SECTOR command is shown in Figure 12.

WRITE SECTOR

The WRITE SECTOR command is used to write one or more sectors of data to the disk from the sector buffer. Upon receipt of WRITE SECTOR command, the 82062 WDC checks the CYLINDER NUMBER LOW/HIGH register pair against the internal cylinder position register to see if they are equal. If not, the direction and number of steps calculation is performed and a seek takes place. The WR FAULT and DRDY lines are checked throughout the command.

When the Seek Complete (SC) line is found to be true (with or without an implied seek having occured), the BDRQ signal is made active and the host proceeds to load the buffer. When the 82062 senses BRDY going high, the ID field with the specified cylinder number, head, and sector size is searched for. Once found, WR GATE is made active and the data is written to the disk. It is necessary to resynchronize the write data since a bit cell can extend from 295 nS to 315 nS during a write cycle. If retries are enabled (T = 0), and if the ID field cannot be found within 10 revolutions, automatic scan ID and seek commands are performed. The ID Not Found error bit is set and the command is terminated if the correct ID field is not found within 10 additional revolutions. If retries are disabled, (T = 1), and if the ID field cannot be found within 2 revolutions, the ID Not Found error bit is set and the command is terminated.

During a WRITE MULTIPLE SECTOR command (M = 1), the SECTOR NUMBER register is incremented and the SECTOR COUNT register is decremented. If the BRDY line is asserted after the first sector is transferred from the buffer, the 82062 will transfer the next sector. If BRDY is deasserted, the 82062 will set BDRQ and wait for the host processor to place more data in the buffer. In summary then, the WRITE SECTOR operation is as follows:

When M = 0,1 (WRITE SECTOR)

(1)	**Host:**	Sets up parameters; issues WRITE SECTOR command.
(2)	**82062:**	Sets BDRQ = 1, DRQ = 1.
(3)	**Host:**	Loads sector buffer with data.
(4)	**82062:**	Waits for BRDY = low to high.
(5)	**82062:**	Finds specified ID field; writes sector to disk.
(6)	**82062:**	If M = 0, then set INTRQ = 1; END.
(7)	**82062**	Increment SECTOR NUMBER register; decrement SECTOR COUNT register.
(8)	**82062**	If SECTOR = 0, then set INTRQ = 1; END.
(9)	**82062**	Go to (2).

A flowchart of the WRITE SECTOR command is shown in Figure 13.

SCAN ID

The SCAN ID command is used to update the SECTOR/DRIVE/HEAD, SECTOR NUMBER, and CYLINDER NUMBER LOW/HIGH registers.

After the command is loaded, the Seek Complete (SC) line is sampled until it is valid. The DRDY and WR FAULT lines are also monitored throughout execution of the command When the first ID field is

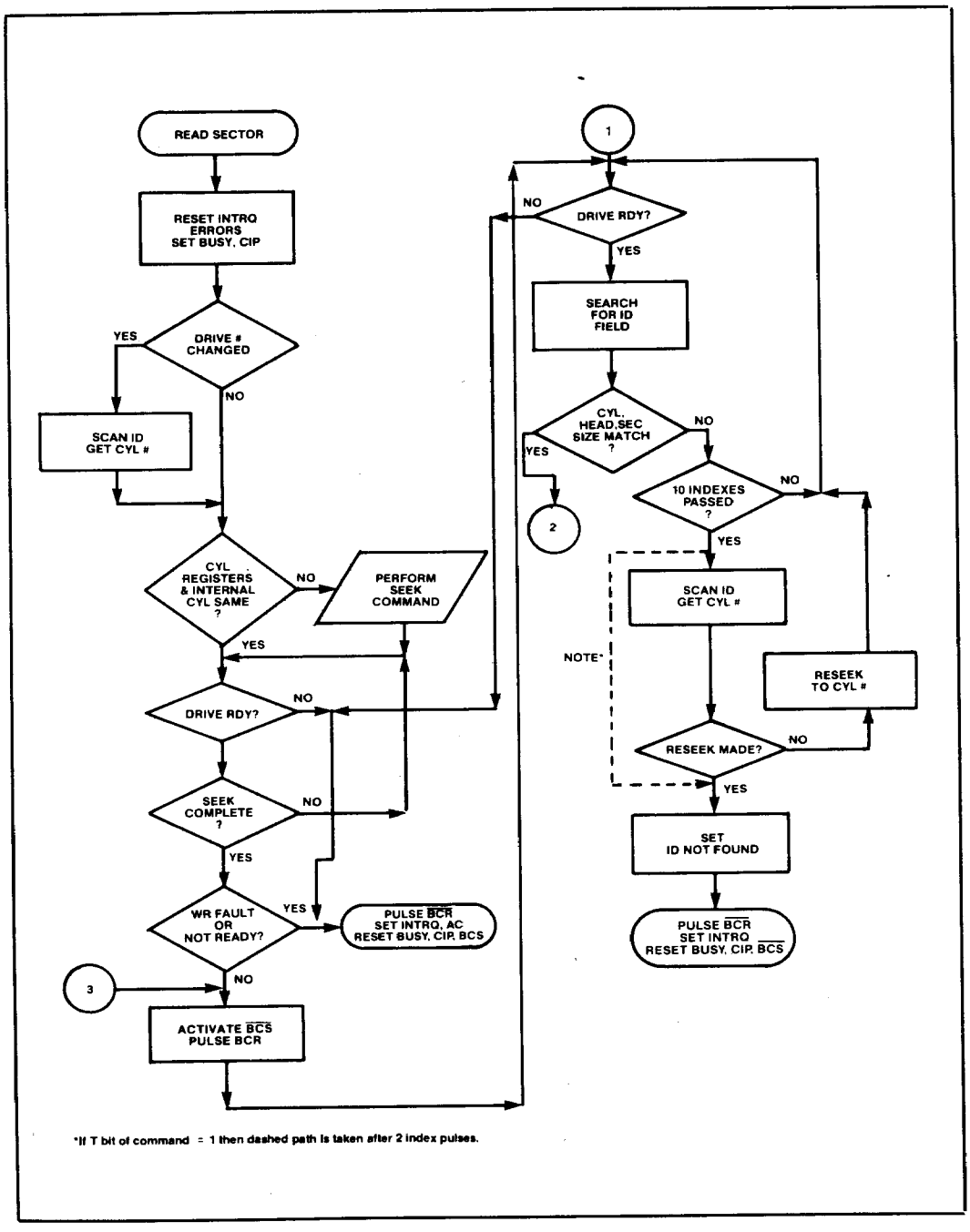


Figure 12A. Read Sector Command Flow

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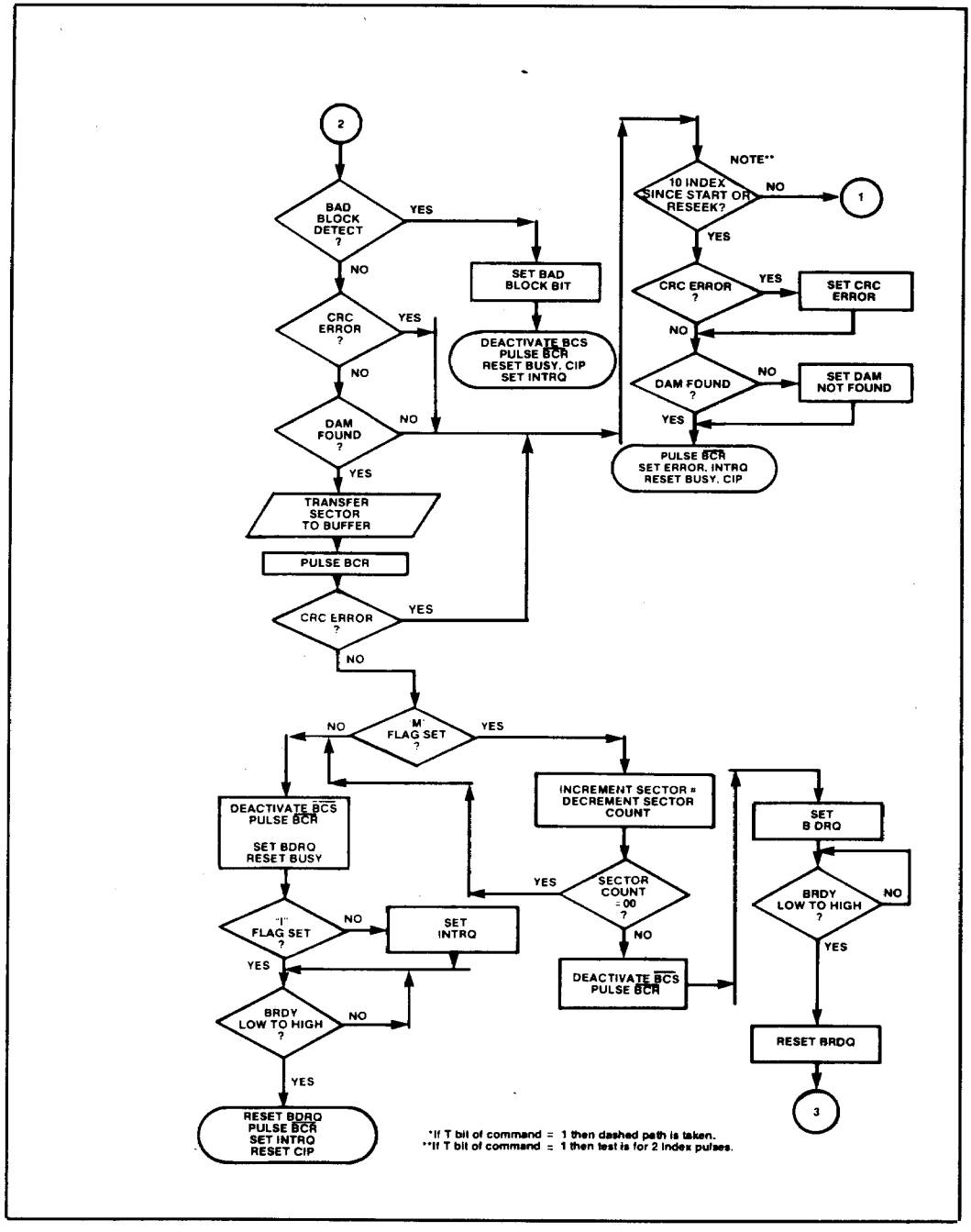

Figure 12B. Read Sector Command Flow

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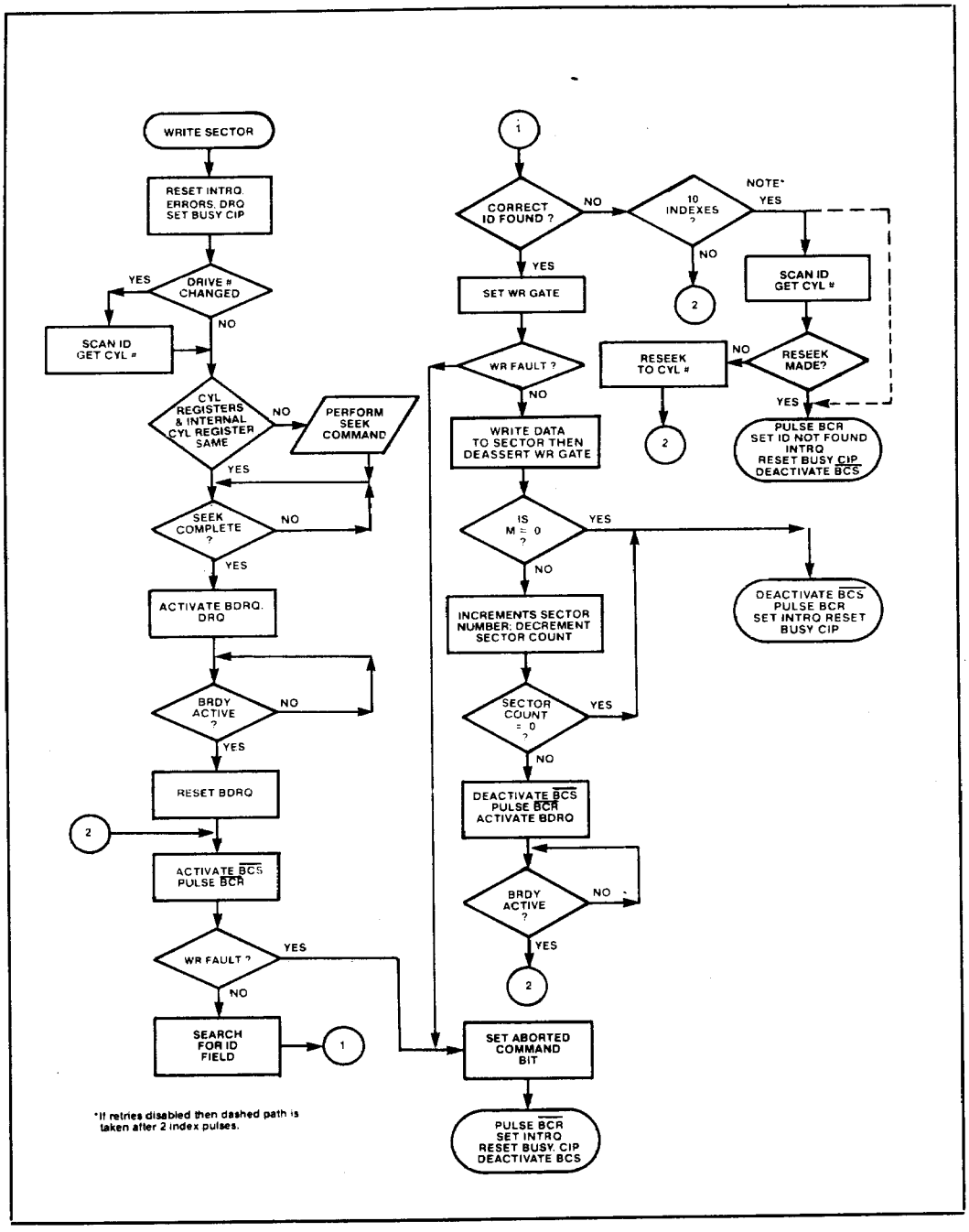

Figure 13. Write Sector Command Flow

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found, the ID information is loaded into the SDH, SECTOR NUMBER, and CYLINDER NUMBER registers. The internal cylinder position register is also updated. If a bad block is detected, the BAD BLOCK bit will also be set. The CRC is checked and if an error is found, the 82062 will retry up to 10 revolutions to find an error-free ID field. There is no implied seek with this command and the sector buffer is not disturbed.

A flowchart of the SCAN ID command is shown in Figure 14.

WRITE FORMAT

The WRITE FORMAT command is used to format one track using the Task Register File and the sector buffer. During execution of this command, the sector buffer is used for additional parameter information instead of sector data. Shown in Figure 15 is the contents of the sector buffer for a 32 sector track format with an interleave factor of two. Each sector requires a two byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. An 00H is normal; an 80H indicates a bad block mark for that sector. In the example of Figure 15, sector 04 will get a bad block mark recorded.

The second byte indicates the logical sector number to be recorded. This allows sectors to be recorded with any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its only purpose is to generate a BRDY to tell the 82062 to begin formatting the track.

An implied seek is in effect on this command. As for other commands, if the drive number has been changed, an ID field will be scanned for cylinder position information before the implied seek is performed. If no ID field can be read (because the track had been erased or because an incomplete format had been been used), an ID Not Found error will result and the WRITE FORMAT command will be aborted. This can be avoided by issuing a RESTORE command before formatting.

The SECTOR COUNT register is used to hold the total number of sectors to be formatted (FFH = 255 sectors), while the SECTOR NUMBER register holds the number of bytes minus three to be used for Gap 1 and Gap 3; for instance, if the SECTOR COUNT register value is 02H and the SECTOR NUMBER register value is 00H, then 2 sectors are written and 3 bytes of 4EH are written for Gap 1 and Gap 3. The data fields are filled with FFH and the CRC is automatically generated and appended. The sector extension bit in the SDH register should not be set. After the last sector is written the track is filled with 4EH.

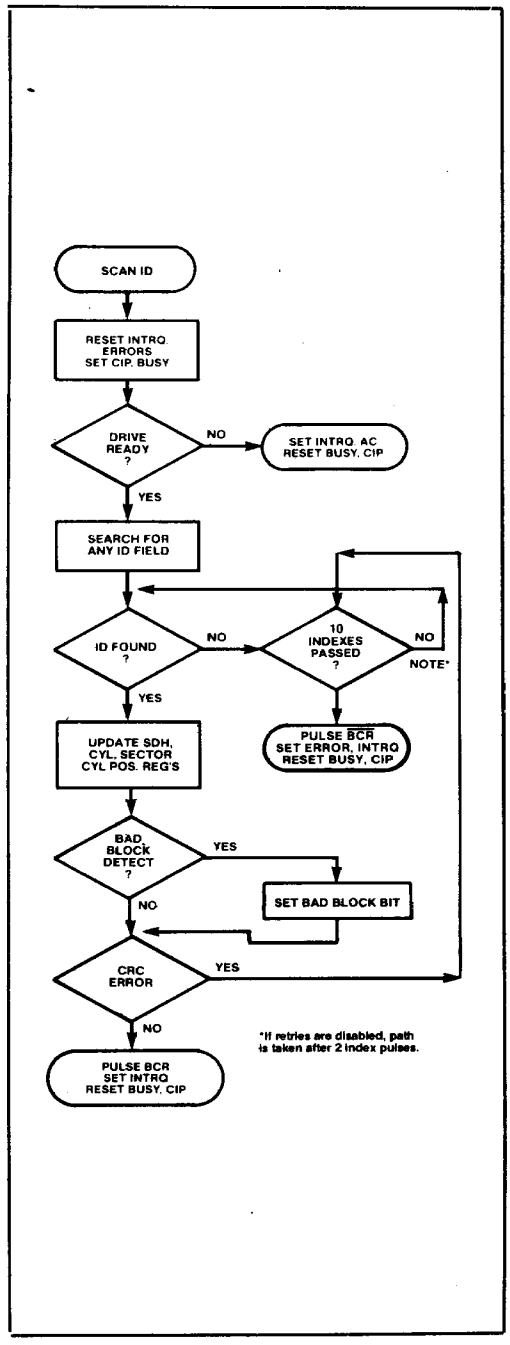

Figure 14. Scan ID Command Flow

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FORMAT COMMAND SECTOR BUFFER CONTENTS

SECTOR BUFFER ADDRESS	BAD BLOCK?	LOCICAL SECTOR NUMBER
00	00	00
02	00	10
04	00	01
06	00	11
08	00	02
0A	00	12
0C	00	03
0E	00	13
10	80	04
12	00	14
14	00	05
16	00	15
18	00	06
1A	00	16
1C	00	07
1E	00	17
20	00	08
22	00	18
24	00	09
26	00	19
28	00	0A
2A	00	1A
2C	00	0B
2E	00	1B
30	00	0C
32	00	1C
34	00	0D
36	00	1D
38	00	0E
3A	00	1E
3C	00	0F
3E	00	1F
40	FF	FF
.	.	.
.	.	.
.	.	.
F0	FF	FF

Figure 15

The Gap 3 value is determined by the drive motor speed variation, data sector length, and the interleave factor. The interleave factor is only important when 1:1 interleave is used. The formula for determining the minimum Gap 3 length value is:

Gap 3 = (2 * M * S) + K + E

M = motor speed variation (e.g., 0.03 for ± 3%)

S = sector length in bytes

K = 25 for interleave factor of 1

K = 0 for any other interleave factor

E = 7 if the sector is to be extended

Like all commands, a WR FAULT or drive not ready condition will terminate execution of the WRITE FORMAT command. Figure 16 shows the format that the 82062 will write on the disk.

A flowchart of the WRITE FORMAT command is shown in Figure 17.

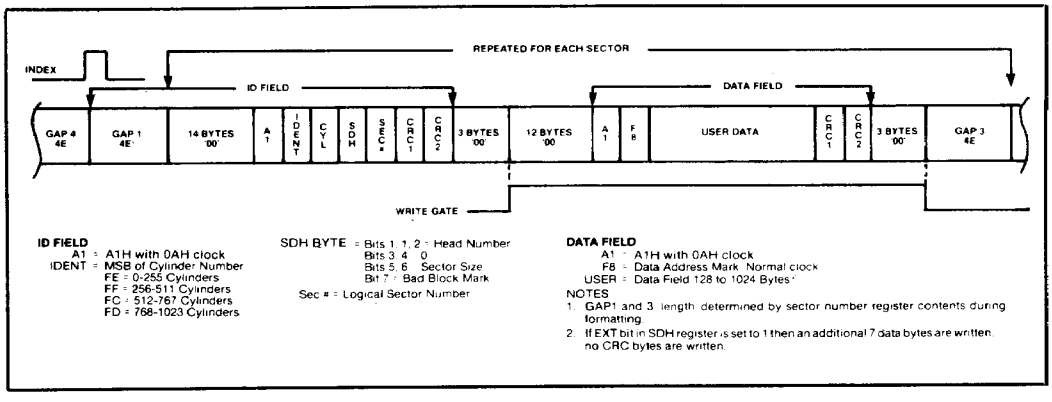

Figure 16. Track Format

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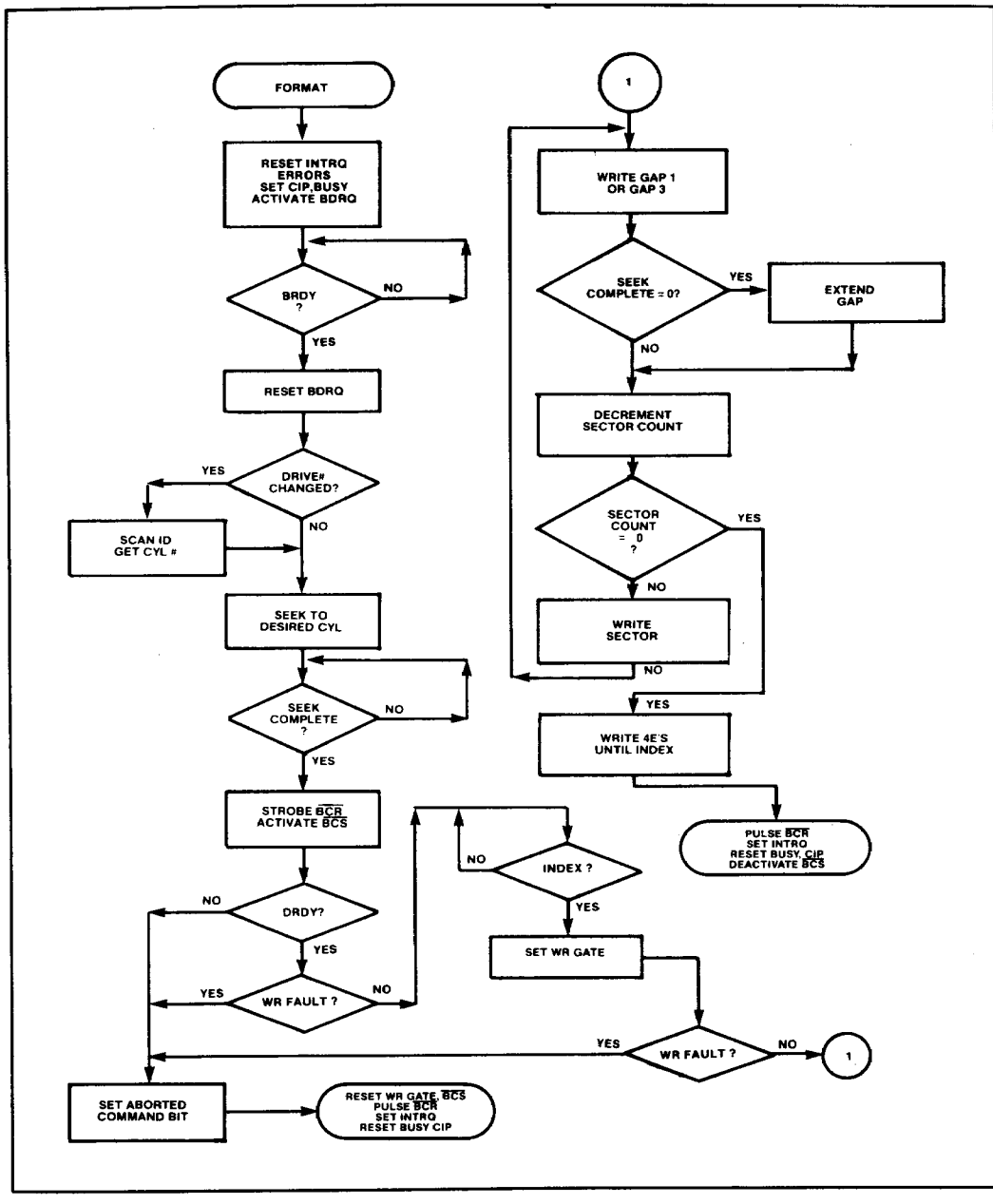

Figure 17. Write Format Command Flow

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ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND ..... -0.5V to +7V
Power Dissipation .....1.5 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

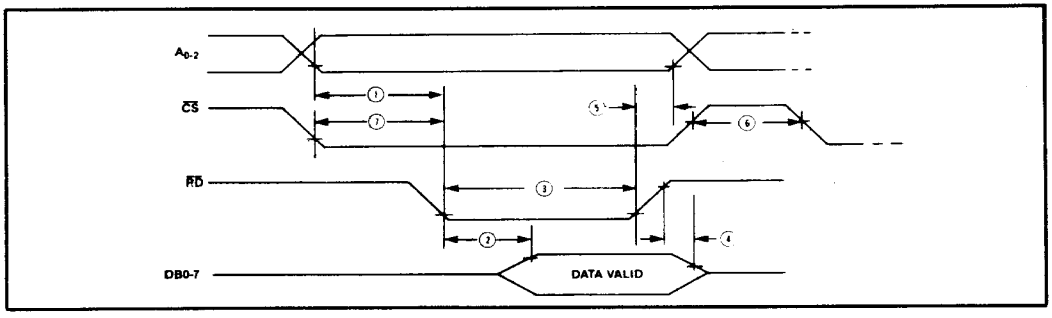
D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = +5V ± 10%; GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
I_{IL}	Input Leakage Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Leakage Current		±10	μA	V_{OUT} = V_{CC} to 0.45V
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100uA
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA 4.8mA P21,22,23
I_{CC}	Supply Current		200	mA	All Outputs Open
C_{IN}	Input Capacitance		10	pF	f_c = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND
	For Pins 25,34,37,39				
V_{IH}	Input High Voltage	4.6		V	
V_{IL}	Input Low Voltage		0.5	V	
TRS	Rise Time		30	ns	10% to 90% points

A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = +5V ± 10%; GND = 0V)

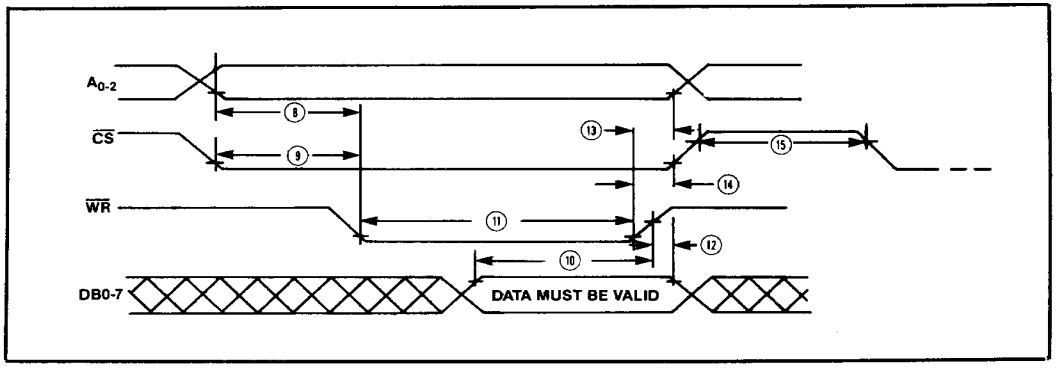
HOST READ TIMING

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
1	Address Stable Before $\overline{RD}$↓	100		ns	
2	Data Delay From $\overline{RD}$↓		375	ns	
3	$\overline{RD}$ Pulse Width	0.4	10	μs	
4	$\overline{RD}$ to Data Floating	20	200	ns	
5	Address Hold Time after $\overline{RD}$↑	0		ns	
6	Read Recovery Time	300		ns	
7	$\overline{CS}$ Stable before $\overline{RD}$↓	0		ns	See Note 6



HOST WRITE TIMING

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
8	Address Stable Before $\overline{WR}$↓	0	10	μs	
9	$\overline{CS}$ Stable Before $\overline{WR}$↓	0	10	μs	
10	Data Setup Time Before $\overline{WR}$↑	0.2	10	μs	
11	$\overline{WR}$ Pulse Width	0.2	10	μs	
12	Data Hold Time After $\overline{WR}$↑	10		ns	
13	Address Hold Time After $\overline{WR}$↑	30		ns	
14	$\overline{CS}$ Hold Time After $\overline{WR}$↑	0		ns	See Note 7
15	Write Recovery Time	1.0		μs	



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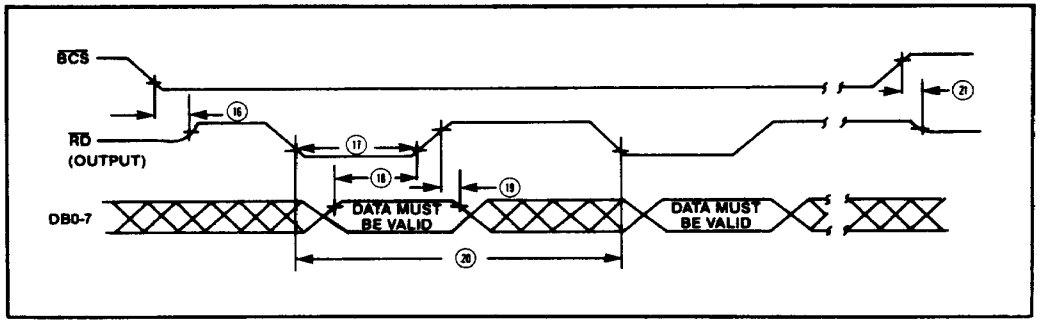
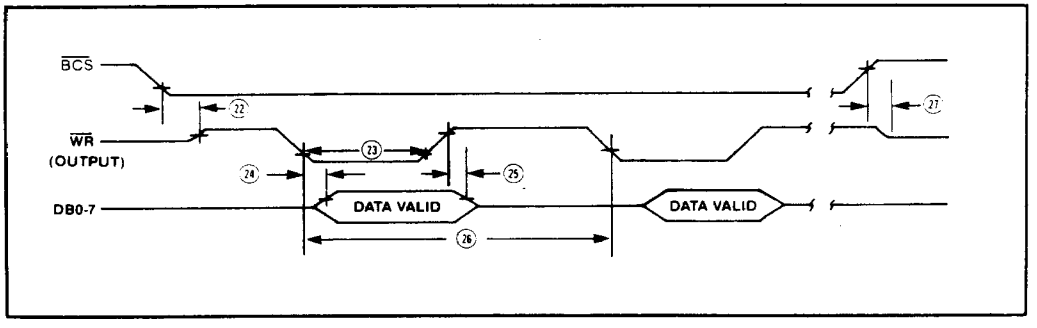
BUFFER READ TIMING (WRITE SECTOR COMMAND)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
16	$\overline{BCS}$↓ to $\overline{RD}$ Valid	15		100	ns	
17	$\overline{RD}$ Output Pulse Width	300	400	500	ns	See Note 3
18	Data Setup to $\overline{RD}$↑	140			ns	
19	Data Hold from $\overline{RD}$↑	0			ns	
20	$\overline{RD}$ Repetition Rate	1.2	1.6	2.0	μs	See Note 1
21	$\overline{RD}$ Float from $\overline{BCS}$↑	15		100	ns	



BUFFER WRITE TIMING (READ SECTOR COMMAND)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
22	$\overline{BCS}$↓ to $\overline{WR}$ Valid	15		100	ns	
23	$\overline{WR}$ Output Pulse Width	300	400	500	ns	See Note 3
24	Data Valid from $\overline{WR}$↑			150	ns	
25	Data Hold from $\overline{WR}$↑	60			ns	
26	$\overline{WR}$ Repetition Rate	1.2	1.6	2.0	μs	See Note 1
27	$\overline{WR}$ Float from $\overline{BCS}$↑	15		100	ns	



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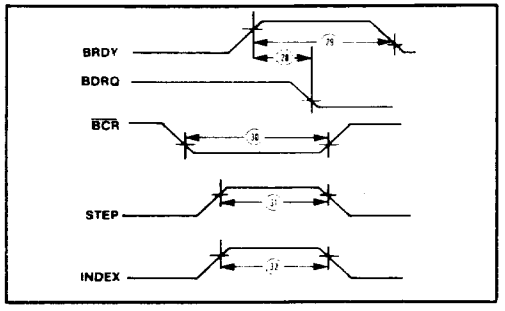
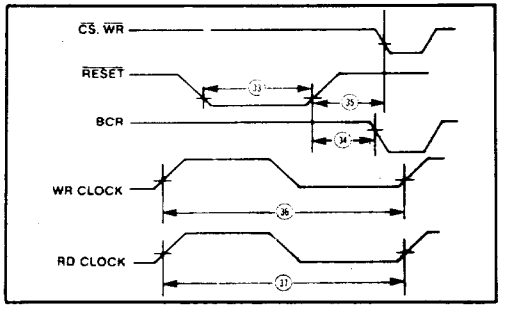
MISCELLANEOUS TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
28	BDRQ Reset from BRDY	40	-	200	ns	
29	BRDY Pulse Width	800			ns	See Note 4
30	$\overline{BCR}$ Pulse Width	1.4	1.6	1.8	μs	See Note 1
31	STEP Pulse Width	8.3	8.4	8.7	μs	See Note 1
32	INDEX Pulse Width	500			ns	
33	$\overline{RESET}$ Pulse Width	24			WR CLK	See Note 2
34	$\overline{RESET}\uparrow$ to $\overline{BCR}$	1.6	3.2	6.4	μs	See Note 1
35	$\overline{RESET}\uparrow$ to $\overline{WR}$, $\overline{CS}\downarrow$	6.4			μs	See Note 1
36	WR CLOCK Frequency	0.25	5.0	5.25	MHz	50% Duty Cycle
37	RD CLOCK Frequency	0.25	5.0	5.25	MHz	50% Duty Cycle See Note 5





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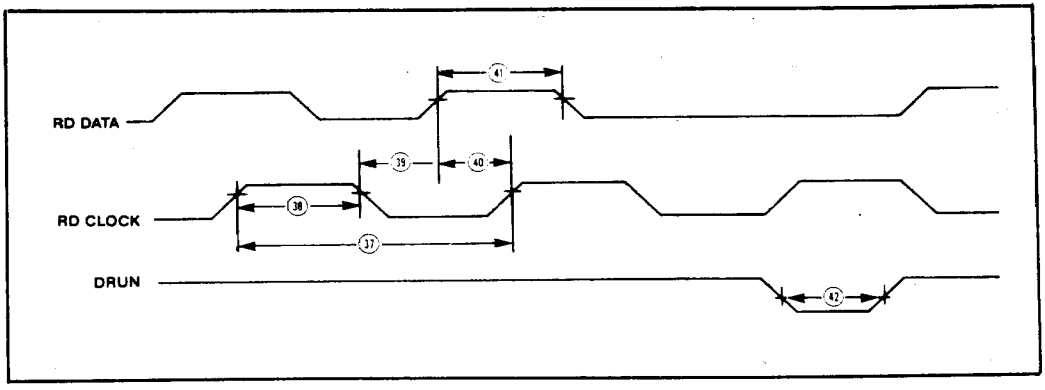
READ DATA TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
38	RD CLOCK Pulse Width	95		2000	ns	50% Duty Cycle
39	RD DATA after RD CLOCK↓	0		T38	ns	
40	RD DATA before RD CLOCK↑	20		T38	ns	
41	RD DATA Pulse Width	40		T38	ns	
42	DRUN Pulse Width	30			ns	



WRITE DATA TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
43	WR CLOCK Pulse Width	95		2000	ns	
	Propogation Delay					
44A	WR CLOCK↑ to WR DATA↑	10		65	ns	
44B	WR CLOCK↓ to WR DATA↓					
44D	WR CLOCK↓ to WR DATA↑					
45A	WR CLOCK↑ to $\overline{\text{EARLY/LATE}}$↓	10		65	ns	
45B	WR CLOCK↓ to $\overline{\text{EARLY/LATE}}$↑					
46A	WR CLOCK↑ to $\overline{\text{EARLY/LATE}}$↑	10		65	ns	
46B	WR CLOCK↓ to $\overline{\text{EARLY/LATE}}$↓					

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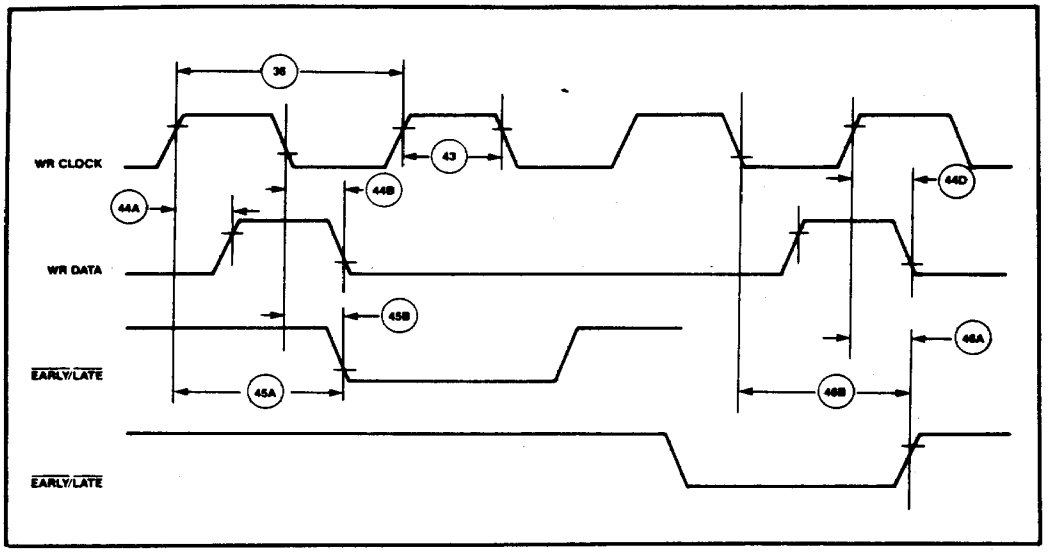
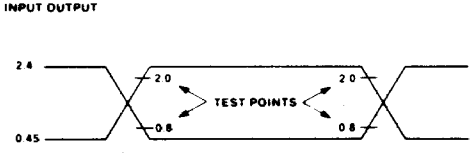
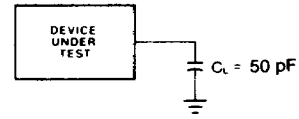


A.C. TESTING INPUT, OUTPUT WAVEFORM



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1, AND 0.45V FOR A LOGIC .0. TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC 1, AND0.8V FOR A LOGIC .0.

A.C. TESTING LOAD CIRCUIT



C_L INCLUDES JIG CAPACITANCE

NOTES:
1. Based on WR CLOCK = 5.0 MHz.
2. 24 WR CLOCK periods = 4.8 μs at 5.0 MHz.
3. 2 WR CLOCK periods ± 100 ns.
4. When used with a DMA controller BRDY must be > 4 μs or a spurious BDRQ pulse may exist for up to 4 μs after the rising edge of BRDY.
5. $\overline{WR}$ CLOCK Frequency = $\overline{RD}$ CLOCK Frequency ± 15%.
6. $\overline{RD}$ may be asserted before $\overline{CS}$ as long as it remains active for at least the minimum. T3 pulse width after $\overline{CS}$ is asserted.
7. $\overline{WR}$ may be asserted before $\overline{CS}$ as long as it remains active for at least the minimum T11 pulse width after $\overline{CS}$ is asserted.

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